Amendments to the Specification

Please replace the second paragraph on page 1, with the following amended paragraph:

1 x 2 splitters in the form of adiabatic Y-junction or Y-branch waveguide structures are well known and used in planar lightguide circuits (PLCs). Fig. 1 shows a conventional y-branch splitter in which a single-mode input waveguide 1 branches into two single mode output waveguide 2,3 at a Y-junction 4. Where the branching ratio is 1:1 we call this a symmetric Y-branch. Such Y-branch structures can be arranged in a cascaded arrangement to form a $1x2^N$ splitter, as illustrated in Fig.3 (which shows a 1 x 16 splitter). A problem with the Y-branches is that it is very difficult in practice to fabricate a perfect point 5 in the Y-junction, where the two output waveguides 2,3 meet. In practice, instead of a perfect point, a flat edge or "blunt" 6 is formed, as shown in Fig 2. In fact, in order to meet required manufacturing tolerances in order to make a ~~reproducable~~ reproducible device, the splitter will commonly be purposely designed to have the blunt taper shape 4 shown in Fig.2. A disadvantage of this blunt is that radiation modes are excited at the blunt, leading to insertion loss. In a $1x2^N$ splitter such as shown in [[Fig. 2]] Fig. 3 the insertion loss at each Y-branch may add up to an unacceptably high total insertion loss (IL) in the splitter device. Moreover, the generation of radiation modes results in reduced Insertion Loss uniformity (ILU) i.e. the variation of the IL as a function of wavelength, across the operational wavelength range of the device.

Please replace the fourth paragraph beginning on page 4 and continuing on page 5, with the following amended paragraph:

Fig.5 illustrates a 1 x 2 splitter formed in a Planar Lightguide Circuit (PLC) chip 18. The splitter comprises a single-mode input waveguide 20 coupled to two output waveguides 24,26 by

a non-adiabatic tapered waveguide 22. The output waveguides each consist of a single mode waveguide having an adiabatically tapered end portion 25,27 coupled to the wide (output) end 23 of the non-adiabatic tapered waveguide 22, such that the output waveguides widen towards the non-adiabatic tapered waveguide, 15 in plan view of the splitter as shown in Fig. 5. As can be seen in Fig.5, the taper shape is such that the width of the waveguide 22 gradually increases, in a generally non-linear manner, from the input end 21 coupled to the input waveguide 20, to the output end 23 coupled to the two output waveguides. Where this splitter is the first optical circuit feature on the PLC chip 18, as shown in Fig.5, an input end 19 of the input waveguide 20 will abut the input face 17 of the PLC chip. The taper shape of the non-adiabatic tapered waveguide 22 is generally designed to cause continuous mode conversion, of the fundamental mode to the second order mode, of an input signal entering the input end 21 of the tapered waveguide from the input waveguide 20, along the length L of the taper 22, to form a double-peaked mode field at the output end 23 of the taper 22. In the embodiment of Fig. 5, the shape of the non-adiabatic tapered waveguide is based on a perturbed cosine function, and is defined by the following equations (with reference to Fig -6):

~~$w(t) = w_{in} + \frac{w_{out} - w_{in}}{2}[1-\cos(2\pi t)]$~~

$$w(t) = w_{in} + \frac{w_{out} - w_{in}}{2}[1-\cos(\pi t)]$$

$$z(t) = L\left[t + \frac{p}{2\pi}\sin(2\pi t)\right]$$

$$t = [0..1]$$

where L is the length of the non-adiabatic tapered waveguide 22;

w(t) is the width along the propagation direction;

z(t) is the length along the propagation direction;

w_{in} and w_{out} are the widths of the input and output ends 21,23 respectively of the tapered waveguide 22; and p is a shape factor, which preferably has a value between 0 and 1, most preferably between 0.6 and 0.9, and which basically controls the slope in the middle (z=0.5L) of the taper (values of p greater than 1 are also possible, though less 10 preferred).

Please replace the second paragraph beginning on page 7 and continuing on page 8, with the following amended paragraph:

In known manner the waveguides in the PLC chip 18 are all typically formed as silica "cores" 32 on a silicon substrate 30 (an oxide layer 3 1 is commonly provided on the substrate prior to depositing the waveguide materials and/or a lower silica cladding layer [[31]] (not shown) may be deposited) and are covered in a cladding material 34, using Flame Hydrolysis Deposition (FHD) or Chemical Vapour Deposition (CVD) fabrication processes (together with photolithography and etching steps). Fig. 9 shows one such waveguide formed in a PLC chip 40. However the present invention is equally applicable to waveguide devices formed in other material systems, or having a different waveguide structure e.g. rib waveguides.

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